Electronic Version
Stylesheet Version v1.1.1

# Description

# [FREQUENCY SYNTHESIZING AND BACK-END PROCESSING CIRCUIT AND METHOD THEREOF]

## CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 93102108, filed on January 30, 2004.

## BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] This invention generally relates to a frequency synthesizing and back-end processing circuit and method thereof, and more particularly to a digital frequency synthesizing circuit including a linear feedback shift register, logic units, and an analog or digital mixer and a filter for back-end processing.

[0004] Description of Related Art

[0005] In the conventional art, there are several frequency synthesizers such as direct frequency synthesizer, phase lock

loop frequency synthesizer, and digital frequency synthesizer. Generally, a frequency synthesizing circuit for back-end processing includes a phase lock loop, a mixer, and a filter. FIG. 1 is a conventional back-end processing circuit 100. Referring to FIG. 1, this circuit includes phase lock loop (102, 104, 106), a mixer (108), and a filter (110). The phase lock loop (PLL) includes phase detector 102, a low pass filter (LPF) 104, and a voltage controlled oscillator (VCO) 106. The PLL up-converts the received signal to a RF signal. The mixer 108 mixes the RF signal with the local oscillation frequency. The filter 110 then filters the mixed signal to obtain the synthesized frequency.

[0006] However, the conventional art has some drawbacks. First, the PLL is not a low power consuming device because it requires a relatively long period to transmit the precise frequency. Further, generally an analog circuit designer has to make a choice between signal stability and phase locking time, which usually causes a lose-lose situation. In addition, an analog circuit usually has fabrication migration issue and the quality of the signal will be affected due to the choice of the loop phase bandwidth of the analog PLL.

[0007] Hence, the present invention provides a fully digital fre-

quency synthesizer and a more flexible back-end processing circuit, by using a digital circuit with a simplified analog circuit, to avoid the issue generated by the analog PLL.

## SUMMARY OF INVENTION

[0008] The present invention is related to a fully digital frequency synthesizer.

[0009] According to an embodiment of the present invention, a back-end processing circuit is attached to the frequency synthesizer.

[0010] According to an embodiment of the present invention, the circuit with fully digital frequency synthesizer is provided by using interpolation and a linear feedback shift register (LFSR). The frequency synthesizer stores the binary data of two frequencies in a shift register and uses interpolation to synthesize a frequency ranged between two predetermined frequencies. The frequency resolution determined by the number of the stages of the LFSR.

[0011] The frequency synthesizer, in accordance with an embodiment of the present invention, uses two memory units to store two reference frequencies such as f1 and f2 in a form of a digital sequence. Theoretically, all frequencies ranged between these two reference frequencies can be

synthesized by this structure of the present invention. The max resolution is $|f_1-f_2|/2^N$, wherein N is the number of the stages of the LFSR. The multiplexer in the frequency synthesizer is determined by a target value. The comparison result between the target value and a predetermined value will determine one of the two stored reference frequencies passes through the multiplexer. After the comparison is complete, the value in the LFSR will shift one bit and then the comparison repeats again. The frequency synthesizer consists of fully digital circuits and operates based on a system clock signal. Therefore, the frequency synthesizer of the present invention can achieve a high frequency resolution with a lower circuit complexity.

[0012] The synthesized frequency is a series of a binary digital sequence and is processed by a digital-to-analog converter so that the frequency synthesizer can provide digital and analog synthesized frequencies at the same time. If analog synthesized frequency is selected, the back-end processing circuit will use voltage controlled oscillator to mix the frequency. If digital synthesized frequency is selected, the back-end processing circuit will use numerical controlled oscillator to mix the frequency. Finally, the mixed frequency will be processed by a filter. This filer

can be a low pass filter, a band pass filter, or a high pass filter. Also, the filter can be designed as a digital filter or an analog filter depending on the users need.

[0013] In an embodiment of the present invention, the frequency synthesizer can provide a high frequency resolution with a lower circuit complexity.

[0014] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

## Brief Description of Drawings

[0015] FIG. 1 is a conventional back-end processing circuit 100.

[0016] FIG. 2 is a block diagram of the frequency synthesizing and back-end processing circuit in accordance with an embodiment of the present invention.

## Detailed Description

[0017] FIG. 2 is a block diagram of the frequency synthesizing and back-end processing circuit in accordance with a preferred embodiment of the present invention.

[0018] The basic structure of the frequency synthesizer is shown

in FIG. 2, wherein 'Seq. +' 202 and 'Seq. −' 204 are two memory units for storing the digital sequence of the reference frequencies f1 and f2 in the two sinusoidal waves $\sin(2\pi f_1 t)$ $\sin(2\pi f_2 t)$, for example, a binary sequence. These two reference frequencies are generated by reference system frequency. Theoretically, all frequencies ranged between these two reference frequencies can be synthesized by this structure of the present invention. The max resolution is $|f_1 - f_2|/2^N$, wherein N is the number of the stages of the LFSR 206, i.e., the number of the shift registers in the LFSR. For example, to generate a binary digital sequence with a system frequency 13.392MHz, the two reference frequencies can be set as 11393/66 = 202.909kHz and 119392/67 = 199.881kHz, respectively. Assuming that the desired synthesized frequency is 201kHz, the value in the memory units 'Seq. +' 202 and 'Seq. −' 204 can be represented as "00000000000000011111111111111110000000000000000-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1" and "00000000000000001111111111111110000000000000000-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1". For simplification, these two sequences can be represented as 16/17/16/17 and 17/17/16/17. Because 11392/201 =

66.6269, the probability to transmit the data in 'Seq. +' is 0.6269; hence, the probability to transmit the data in 'Seq. -' is 0.3731 (i.e., 1- 0.6269). If the LFSR 206 has 10 stages, the function generated by LFSR can be represented by a Galois structure $g(D) = 1+D^3+D^{10}$. However, a Fibonacci structure can also be used. In an embodiment of the present invention, the number of the stages of the LFSR is 10. Therefore, the max resolution is $(202.909-199.881)/2^{10} = 0.002957$kHz, and the target frequency can be set as round $(0.3721*1024)/1024 = 0.3730_{(10)} = 0101111110_{(2)}$. The LFSR will pre-store the target frequency. As shown in FIG. 2, the output of the first multiplexer 208 is determined by the control unit 210, which is based on the comparison between the target frequency in the LFSR 206 and the predetermined value. When the target frequency is smaller than the predetermined value, the control unit 210 will select to output the data 231 in 'Seq. +' memory unit 202. When the target frequency is larger than the predetermined value, the control unit 210 will select to output the data 233 in 'Seq. -' memory unit 204. The counter is controlled by the digital clock Digi_clk. After comparing a sequence, the value in the LFSR 206 will be shifted one bit, and the compari-

son will repeat again until the difference between synthesized frequency and the target frequency is smaller than the max resolution. Then a digital synthesized frequency 239 is obtained.

[0019] Then a digital-to-analog converter converts the digital synthesized frequency sequence 239 to an analog frequency signal 241. The second multiplexer 214 can selectively output one of the digital synthesized frequency sequence and the analog synthesized frequency signal, which is selected by the outer source or a user-predetermined control signal OUTPUT_SEL. This selected signal 243 then is sent to a mixer 216. If the digital synthesized frequency is selected, a numerical controlled oscillator will be used to mix the frequency. If analog synthesized frequency is selected, a voltage controlled oscillator will be used to mix the frequency. The mixing method is selected by the control signal OUTPUT_SEL.

[0020] Further, the mixed signal 245 is sent to a filter 218 to remove the noise. Here, the frequency synthesizing and back-end processing is complete. In an embodiment of the present invention, the filter can be a low pass filter, a band pass filter, or a high pass filter.

[0021] The above description provides a full and complete de-

scription of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.